REMARKS

The Official Action dated February 7, 2005 has been received and its contents carefully noted. In view thereof, claim 2 has been canceled and claims 1, 3, 4, 5, 7 and 9 have been amended in order to better define that which Applicants regard as the invention. Accordingly, claims 1 and 3-9 are presently pending in the instant application.

Initially, Applicants wish to acknowledge the Examiner's indication on page 6 of the Office Action that claim 4 is allowable over the prior art of record and that claims 7-9 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. §112, second paragraph as set forth in the Office Action. As can be seen from the foregoing amendments, independent claim 7 has been amended in order to overcome the rejection under 35 U.S.C. §112, second paragraph as set forth by the Examiner. Accordingly, it is respectfully submitted that claims 7-9 are now in proper formal condition for allowance.

With reference to page 2 of the Office Action, the title of the invention has been objected to as not being descriptive. As can be seen from the foregoing amendments, the title suggested has been adopted and consequently it is respectfully submitted that the title of Applicants' application is now clearly descriptive of the claimed invention.

With reference to paragraph 6 of the Office Action, claims 7-9 have been rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner notes in claim 7, lines 22 and 23 that the phrase "or applying the ground voltage to the other end of said load resistance and the ground voltage to said reset line" is unclear and consequently there would not be any current flow between the bit line. As can be seen from the foregoing amendments, independent claim 7 has been amended to properly recite that "applying the ground voltage to the other end of said load resistance and the power voltage to

said reset line". Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 7 as well as those claims which depend therefrom are now in proper formal condition for allowance.

With reference now to paragraph 8 of the Office Action, claims 1-3 and 5-6 have been rejected under 35 U.S.C. §102(a)/(e) as being anticipated by U.S. Patent No. 6,151,242 issued to Takashima. This rejection is respectfully traversed in that the patent to Takashima neither discloses nor suggests that which is presently set forth by Applicants' claimed invention.

With respect to independent claim 1, this claim is directed to a method for driving a semiconductor memory wherein the voltage applied to the set line or the reset line for writing or erasing data in the selected ferroelectric capacitor is the power voltage or the ground voltage.

As the Examiner can readily appreciate, Takashima discloses in Figs. 9 and 10 that when a data is written or rewritten after destructive read-out, the data is transferred from the bit line to the sub bit line through the transistor Q7. In this case, the transistor Q6 is turned off. Therefore, unlike the present invention, VSE (reset line) in Takashima is not at all related to writing or rewriting of the data. That is, the reset line in Takashima does not participate in writing a data whereas the reset line in accordance with the present invention clearly participates in the writing or erasing of data.

Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 1 wherein the voltage applied to the set line and the reset line for writing or erasing a data in the selected ferroelectric capacitor are the power voltage or the ground voltage which is clearly neither disclosed in nor remotely suggested by the teachings of Takashima. Consequently, it is respectfully submitted that independent claim 1 is now in proper condition for allowance.

With respect to independent claim 3, this claim recites a method for driving a semiconductor memory wherein the potential differences caused between an upper electrode and a lower electrode of the selected ferroelectric capacitor by subtracting a ground voltage that is applied to the reset line from a power voltage that is applied to a set line, in writing a data in the selected ferroelectric capacitor. Again, it is respectfully submitted that the patent to Takashima neither discloses nor remotely suggests these features.

Particularly, the voltage in Takashima that is applied to the ferroelectric capacitor is a potential difference caused by subtracting the ground voltage that is applied to /PLB, which is a different line from VSE as the reset line, from the power voltage that is applied to /PLA as noted in Fig. 9. Further, it is noted from the Examiner's rejection of independent claim 1 that the Examiner agrees that /PLA is a set line and VSA is a reset line. Consequently, the ground voltage is not applied to the reset line in Takashima. Accordingly, it is respectfully submitted that Applicant's claimed invention as set forth in independent claim 3 is clearly neither disclosed in nor suggested by the method taught by Takashima. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 3 is now in proper condition for allowance.

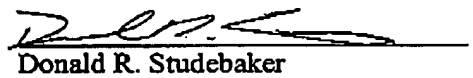
With respect to independent claim 5, as can be seen from the foregoing amendments, independent claim 5 recites a method for driving a semiconductor memory wherein the reading voltage is set to such a magnitude that the potential difference does not exceed the coercive voltage of the selected ferroelectric capacitor in reading a data in the selected ferroelectric capacitor. In doing so, in accordance with the invention as set forth in independent claim 5, polarization of the ferroelectric capacitor does not invert when reading a data. It is noted that Takashima discloses in column 34, lines 15 and 16 that polarization inversion takes place when reading a data. Clearly, this is directly contrary to that which is

presently set forth by Applicants' claimed invention wherein the reading voltage that is applied is set so as not to exceed the coercive voltage of the ferroelectric capacitor and thus polarization of the ferroelectric capacitor does not invert when reading a data. Therefore, it is assured that displacement of polarization of a ferroelectric film returns to the displacement before the readout of the data, when the reading voltage that is applied to the set line is erased. Accordingly, in that the Takashima reference discloses a method which is directly contrary to that set forth by Applicants' claimed invention, that is causing polarization inversion of the ferroelectric capacitor, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 5 clearly distinguishes over the teachings of Takashima and thus claim 5 as well as claim 6 which depends therefrom clearly distinguish over the teachings of Takashima and are in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1 and 3-9 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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